Chapter 3

Diodes, Problem Solutions

3.1 Problem 3.13

A square wave of 10 V peak-to-peak amplitude and zero average is applied to a circuit resembling that in Figure (3.1) and employing a 100 Ω resistor. Assuming an ideal diode what is the peak output voltage that results? What is the peak diode current? What is the average diode current? What is the maximum reverse voltage across the diode?

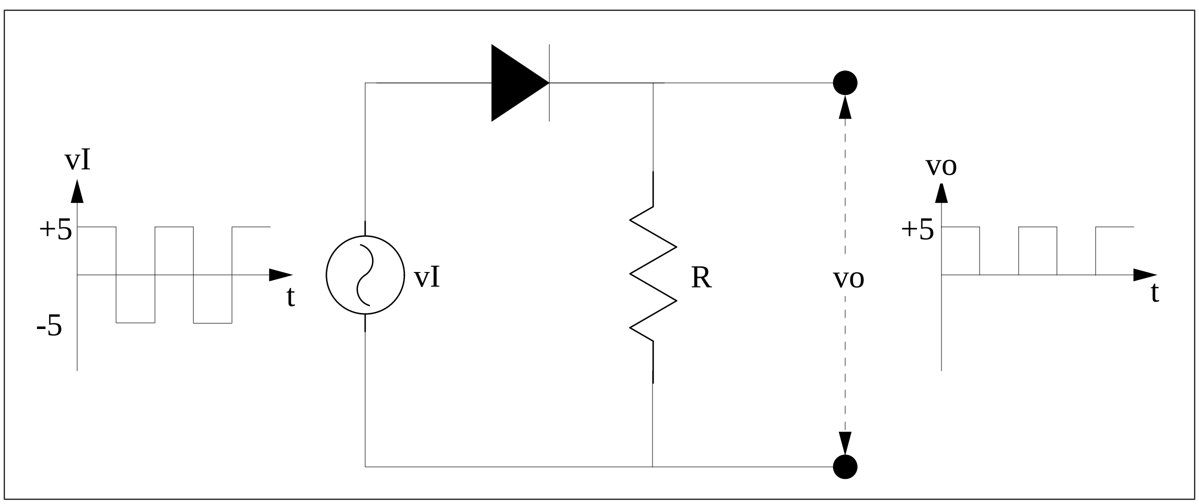

Figure 3.1:

Solution

The peak output voltage $\hat{v}_o$ is:

$$\hat{v}_o = 5\ V$$

However $v_o(t)$ is given by:

$$\begin{array}{lllllll} v_o(t) & = & 5 & 0 & \leq & t & \leq & T/2 \\ v_o(t) & = & 0 & T/2 & < & t & \leq & T \end{array}$$

Let the period of the input voltage be T, then the average out output voltage v_{oavg}:

$$\begin{aligned} v_{oavg} &= \frac{1}{T}\int_o^T v(t)\ dt \\ &= \frac{1}{T}\left[\int_0^{T/2} v_o(t)\ dt + \int_{T/2}^{T} v_o(t)\ dt\right] \\ &= \frac{1}{T}\left[\int_0^{T/2} 5\ dt + \int_{T/2}^{T} 0 \times\ dt\right] \\ &= \frac{5}{T}\int_0^{T/2} dt \\ &= \frac{5}{T} \times \frac{T}{2} \\ &= 2.5\ V \end{aligned}$$

The peak and average currents $\hat{i}$ and i_{avg} are given by:

$$\begin{aligned} \hat{i} &= \frac{\hat{v}_o}{R} \\ &= \frac{5}{100} \\ &= 50\ mA \\ i_{avg} &= \frac{v_{oavg}}{R} \\ &= \frac{2.5}{100} \\ &= 25\ mA \end{aligned}$$

Maximum reverse voltage is 5 V.

3.2 Problem 3.27

The circuit shown in Figure (3.2) uses identical diodes for which $I_D = 1$ mA at $V_D = 0.7$ V with $n = 1$. At $20°C$, voltage V is measured by a very high resistance meter to be 0.1 V. By what factor does the reverse leakage current of these diodes exceed I_s? Estimate the value of V when the temperature is raised by $50°C$.

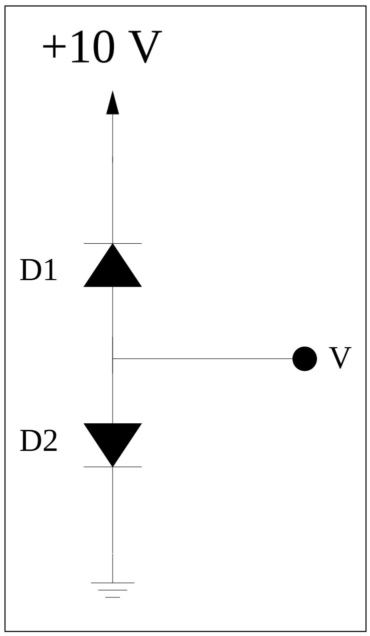

Figure 3.2:

Solution

The diode reverse leakage current $I_D = 1$ mA is defined by:

$$
\begin{aligned}
I_D &= I_s e^{V_D/V_T} \\
10^{-3} &= I_s e^{0.7/0.025} \\
I_s &= 10^{-3} \times e^{-0.7/0.025} \\
&= 10^{-3} \times e^{-28} \\
&= 6.91 \times 10^{-16}\ A
\end{aligned}
$$

At $V = 0.1$ V, I_D is:

$$
\begin{aligned}
I_D &= I_s e^{0.1/0.025} \\
&= I_s e^4 \\
&= I_s \times 54.6 \\
\frac{I_D}{I_s} &= 54.6
\end{aligned}
$$

The reverse leakage current doubles for every $10°C$ rise, so for a $50°C$ rise the current increases by a factor of 2^5. I_S doubles for every $5°C$ rise, so for a $50°C$ rise I_s increases by a factor of 2^{10}. we then have:

$$
\begin{aligned}
I_D &= I_s e^{V/V_T} \\
2^5 \times I_D &= 2^{10} \times I_s e^{V/V_T} \\
V &= V_T \ln\left[\frac{2^5 \times I_D}{2^{10} \times I_s}\right] \\
&= 0.025 \ln\left[\frac{54.6}{2^5}\right] \\
&= 0.025 \times \ln(1.706) \\
&= 13.4\, mV
\end{aligned}
$$

3.3 Problem 3.44

Calculate the built-in voltage of a junction in which the p and n regions are doped equally with $10^{16} atoms/cm^3$. Assume the free electron concentration in intrinsic silicon $n_i \simeq 10^5/cm^3$. With no external voltage applied, what is the width of the depletion region, and how far does it extend into the p and n regions? If the the cross sectional area of the junction is 100 μm^2, find the magnitude of the charge stored on either side of the junction, and calculate the junction capacitance C_j.

Solution

The built-in voltage of a $p - n$ junction is given by:

$$\begin{aligned} V_\circ &= V_T \ln \left[\frac{N_A N_D}{n_i^2} \right] \\ &= 0.025 \ln \left[\frac{10^{16} \times 10^{16}}{(10^5)^2} \right] \\ &= 0.025 \times 50.66 \\ &= 1.27\ V \end{aligned}$$

Let W, x_n, x_p and ϵ_s be the total width, the width in the n region, the width in the p region of the depletion region, and the electric permittivity of silicon respectively. W is given by:

$$\begin{aligned} W &= x_n + x_p \\ &= \sqrt{\frac{2\epsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) V_\circ} \\ &= \sqrt{\frac{2 \times 11.7 \times 8.85 \times 10^{-14}}{1.6 \times 10^{-19}} \left(\frac{1}{10^{16}} + \frac{1}{10^{16}} \right) \times 1.27} \\ &= 0.57\ \mu m \end{aligned}$$

Where $\epsilon_s = \kappa \epsilon_\circ$, $\kappa = 11.7$ is the dielectric constant of silicon and $\epsilon_\circ = 8.85 \times 10^{-14}\ F/cm$ is the permittivity of free space.

The ratio of the widths of the depletion region in the n and p regions is given by:

$$\frac{x_n}{x_p} = \frac{N_A}{N_D}$$

Since $N_A = N_D$, then $x_n = x_p = W/2 = 0.28\ \mu m$. Let $A = 100\ \mu m^2$ be the area of the junction, then the charge on the junction $C_j = C_p = C_n$ is given by:

$$\begin{aligned} q_j &= q\frac{N_A N_D}{N_A + N_D} A \times W \\ &= 1.6 \times 10^{-19} \times \frac{10^{16} \times 10^{16}}{10^{16} + 10^{16}} \times 100 \times 10^{-6} \times 0.57 \times 10^{-6} \\ &= 4.56 \times 10^{-14}\ C \end{aligned}$$

The capacitance C_j of the depletion region is given by:

$$\begin{aligned} C_j &= \frac{\epsilon_s A}{W} \\ &= \frac{11.7 \times 8.85 \times 10^{-16} \times 100 \times 10^{-6}}{0.57 \times 10^{-6}} \\ &= 1.82 \times 10^{-12}\ F \\ &= 1.82\ pF \end{aligned}$$

3.4 Problem 3.65

For the circuit shown in Figure (3.3), utilize the constant-voltage-drop model (0.7 V) for each conduction diode and show that the transfer characteristic can be described by:

for -4.65 $\leqslant$ v_I	$\leqslant$	4.65 V	v_o	$=$	v_I
for v_I	$\geqslant$	+4.65 V	v_o	$=$	+4.65 V
for v_I	$\leqslant$	-4.65 V	v_o	$=$	-4.65 V

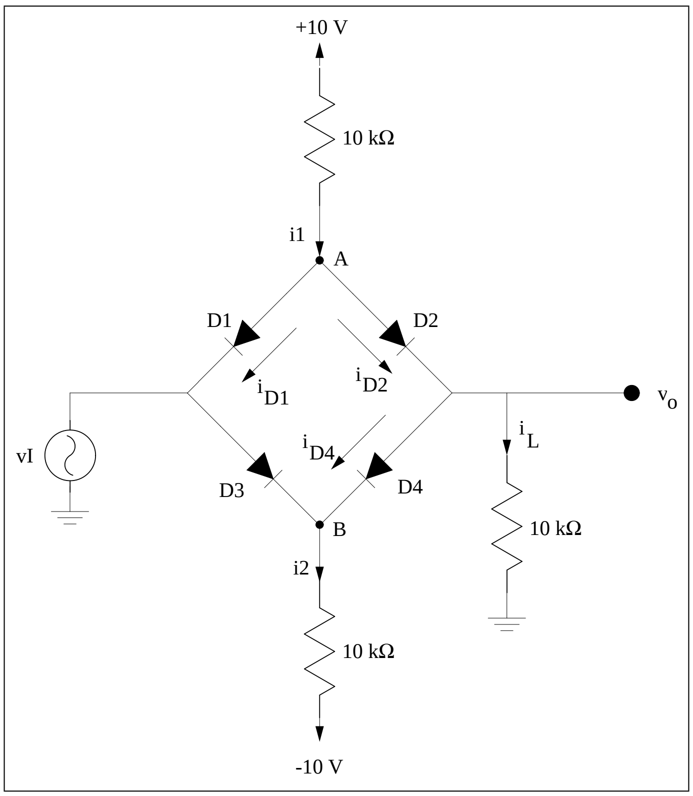

Figure 3.3:

Solution

When V_I is small (close to zero) all four diodes conduct,

$$v_A = v_I + v_{D1}$$

and

$$\begin{aligned} v_o &= v_A - v_{D2} \\ &= (v_I + v_{D1}) - v_{D2} \end{aligned}$$

Since all diodes are identical, and $v_{D1} = v_{D2} = v_{D3} = v_{D4} = 0.7\ V$, then

$$v_o = v_I$$

we also have:

$$v_B = v_I - v_{D3}$$

The currents i_1, and i_L can be calculated as:

$$\begin{aligned} i_1 &= \frac{10 - v_A}{10\ k\Omega} \\ &= \frac{10 - v_I - 0.7}{10\ k\Omega} \\ &= \frac{9.3 - v_I}{10}\ mA \qquad (3.1) \\ i_L &= \frac{v_o}{10\ k\Omega} \\ &= \frac{v_I}{10}\ mA \qquad (3.2) \end{aligned}$$

The current i_1 splits at "A" into i_{D1} and i_{D2}, so $i_{D1} < i_1$, similarly i_{D2} splits into i_L and i_{D4}, so $i_L < i_{D2}$. So, if D_1, D_2, and D_3 conducting, the following inequality must be satisfied:

$$i_L < i_{D2} < i_1$$

Now, as v_I increases in the positive direction i_1 decreases and i_L increases, this means that there will be a valu for v_I at which the above inequality is not satisfied. Under this condition D_1 and D_4 will cut off, $i_{D1} = i_{D4} = 0$ and $i_L = i_{D2} = i_1$. Using Equation (3.1) and Equation (3.2) we can find the value of v_I that makes the three current equal.

$$\begin{aligned} \frac{v_I}{10} &= \frac{9.3 - v_I}{10} \\ v_I &= 9.3 - v_I \\ &= \frac{9.3}{2} \\ &= 4.65\ V \end{aligned}$$

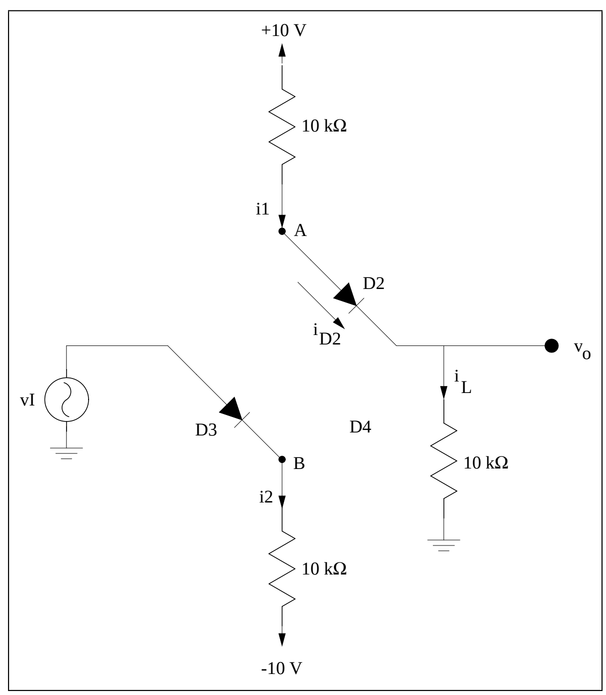

Figure 3.4:

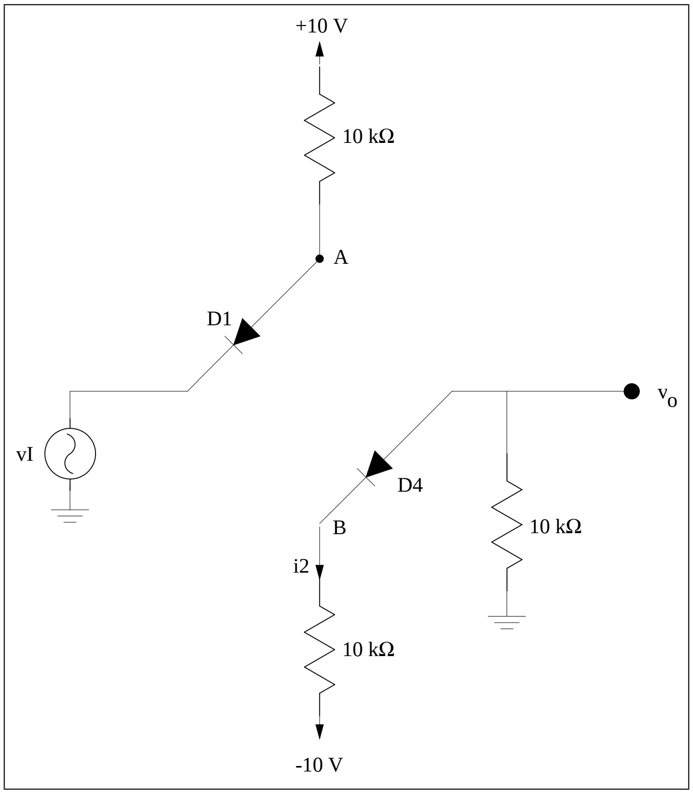

Figure 3.5:

At $v_I = 4.65$ V D_1 and D_4 are cut off while D_3 and D_2 conduct. This situation will continue when $v_I \geqslant 4.65\ V$ and v_o remains constant at +4.65 V as the circuit behave like the one shown in Figure (3.4).

The symmetery of the circuit indicates that a similar limiting value occurs at negative values of v_I spcifically when $v_I \leqslant -4.65\ V$ when D_1 and D_4 conduct and D_2 and D_3 cut off and the circuit reduces to that shown in Figure (3.5).

In conclusion the circuit provides:

$$\begin{array}{lllll} \text{for } -4.65 \leqslant & v_I & \leqslant 4.65 \text{ V} & v_o & = v_I \\ & \text{for } v_I & \geqslant +4.65 \text{ V} & v_o & = +4.65 \text{ V} \\ & \text{for } v_I & \leqslant -4.65 \text{ V} & v_o & = -4.65 \text{ V} \end{array}$$

3.5 Problem 3.70

In the circuit shown in Figure (3.6), I is a dc current and v_s is a sinusoidal signal. Capacitor C is very large; its function is to couple the signal to the diode but block the dc current from flowing into the signal source. Use the diode small-signal model to show that the signal component of the output voltage is:

$$v_o = v_s \frac{nV_T}{nV_T + IR_s}$$

If $v_s = 10\ mV$, find v_o for $I = 1\ mA$, and $1\ \mu A$. Let $R_s = 1\ k\Omega$ and $n = 2$. At what value of I does v_o become one-half of v_s? Note that this circuit function as a signal attenuator with the attenuation factor controlled by the value of the dc current I.

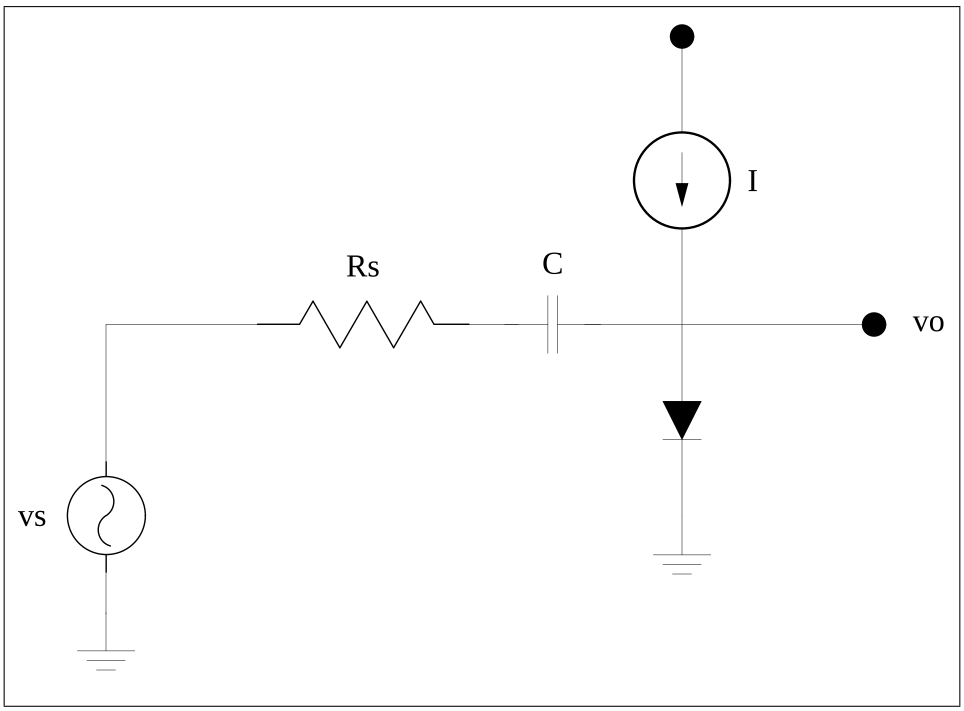

Figure 3.6:

Solution

A large capacitor has a very small reactance to AC signals. The equivalent circuit is shown Figure (3.7), where r_d is the diode resistance. The two resistors in the equivalent circuit

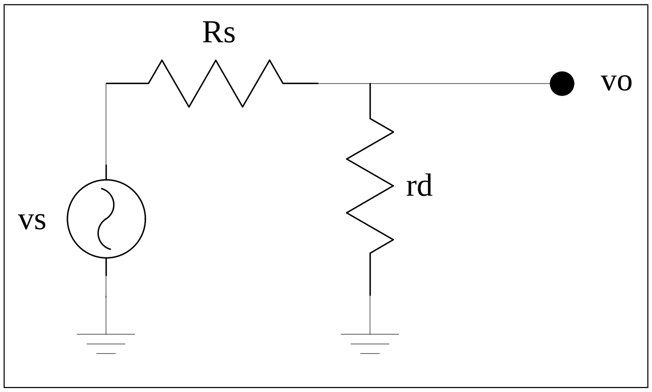

Figure 3.7:

form a voltage divider for the input signal voltage v_s. The output voltage v_o is then given by:

$$v_o = v_s \frac{r_d}{R_s + r_d}$$

since:

$$r_d = \frac{nV_T}{I}$$

then v_o becomes:

$$\begin{aligned} v_o &= v_s \frac{\frac{nV_T}{I}}{R_s + \frac{nV_T}{I}} \\ &= v_s \frac{nV_T}{IR_s + nV_T} \end{aligned}$$

For $v_s = 10\ mV$, $R_s = 1k\Omega$, $n = 2$ and $V_T = 25\ mV$,

$$\begin{aligned} v_o &= 10 \frac{2 \times 0.025}{I + 2 \times 0.025}\ mV \\ &= 10 \frac{0.05}{I + 0.05}\ mV \\ &= 0.5\ mV \qquad \text{for I} = 1\ mA \\ &= 9.8\ mV \qquad \text{for I} = 1\ \mu A \end{aligned}$$

where the current I is in mA.

$$\begin{aligned} \frac{v_o}{v_s} &= \frac{0.05}{I + 0.05} \\ 0.5 &= \frac{0.05}{I + 0.05} \\ I &= 0.05\ mA \\ &= 50\ \mu A \end{aligned}$$

3.6 Problem 3.91

The circuit in Figure (3.8) implements a complementary-output rectifier. Sketch and clearly label the waveforms of v_o^+ and v_o^-. Assume a 0.7 V drop across each conducting diode. If the magnitude of the average of each output is to be 15 V, find the required amplitude of the sine wave across the entire secondary winding. What is the PIV of each diode?

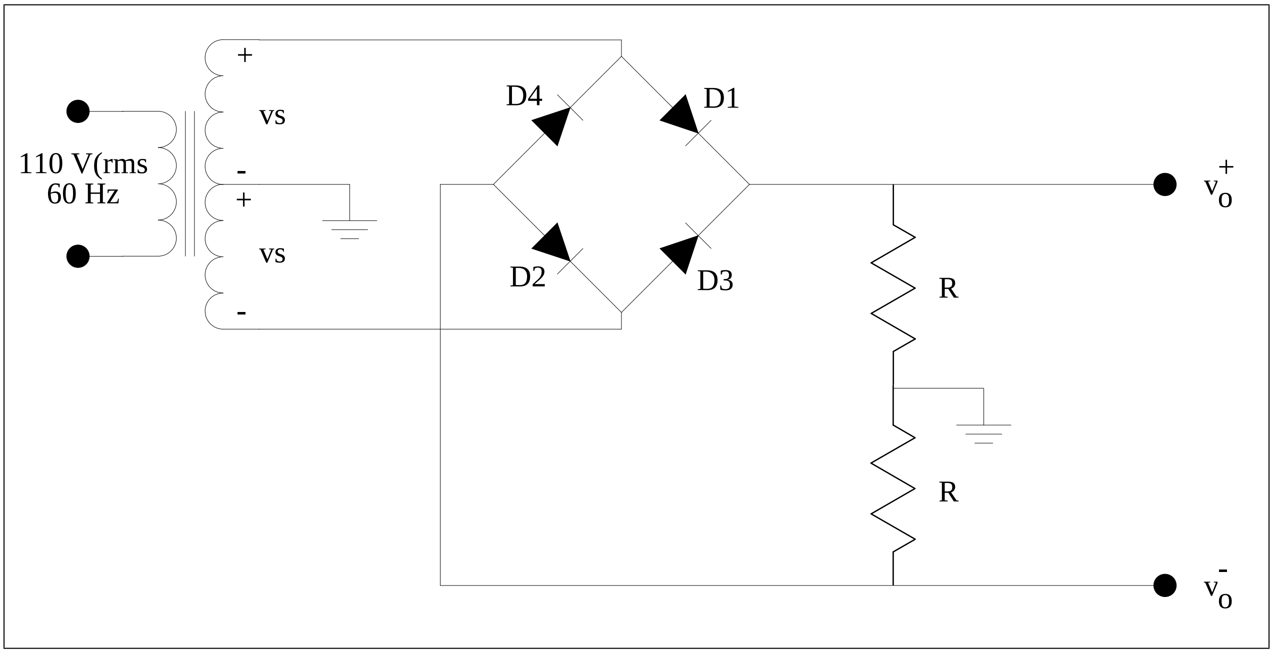

Figure 3.8:

Solution

The voltage at the positive output terminal v_o^+ is given by:

$$
\begin{aligned}
v_o^+ &= v_s \sin(\omega t) - 0.7 && \text{for } \phi \leqslant \omega t \leqslant \pi - \phi \\
&= 0 && \text{otherwise}
\end{aligned}
$$

where ϕ is given by:

$$\phi = \sin^{-1} \frac{0.7}{v_s}$$

The dependence of v_o^+ on ωt is shown in Figure (3.9) for $\phi = 10°$ and $v_s = 15\ V$. The

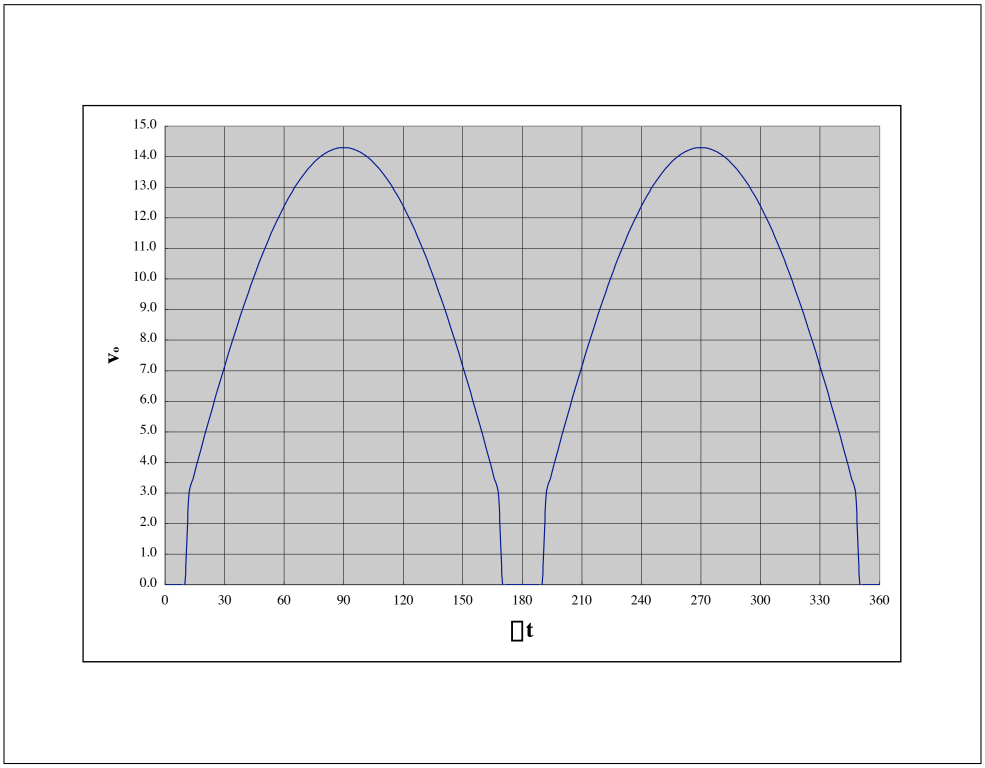

Figure 3.9:

dependence of the voltage of negative output terminal v_o^- on ωt is exactly the same as that of v_o^+ (shown in Figure (3.9)) except that v_o^- is always negative.

The average of v_o^+, is:

$$\begin{aligned}
\overline{v}_o &= \frac{1}{\pi}\int_{\phi}^{\pi-\phi}(v_s\sin\theta - 0.7)d\theta \\
&= \frac{1}{\pi}\left\{v_s\int_{\phi}^{\pi-\phi}\sin\theta\ d\theta - 0.7\int_{\phi}^{\pi-\phi}d\theta\right\} \\
&= \frac{1}{\pi}\left\{v_s\left[-\cos\theta\right]_{\phi}^{\pi-\phi} - 0.7\left[\theta\right]_{\phi}^{\pi-\phi}\right\} \\
&= \frac{1}{\pi}\left\{v_s\left[-\cos(\pi-\phi)+\cos(\phi)\right] - 0.7\left[\pi-\phi-\phi\right]\right\} \\
&= \frac{1}{\pi}\left\{2v_s\cos\phi - 0.7\pi - 1.4\phi\right\}
\end{aligned}$$

If $v_s \gg 0.7$, then $\phi \ll 1$, $\cos\phi \approx 1$ and $1.4\phi \ll 1$ and $\overline{v}_s$ becomes:

$$\overline{v}_o = \frac{2}{\pi}v_s - 0.7$$

We can also have:

$$v_s = \frac{\pi}{2}(\overline{v}_o + 0.7)$$

for $\overline{v}_o = 15\ V$, then $v_s = 24.66\ V$. The required amplitude across the entire secondary windings is $49.32\ V$.

The maximum reverse bias across each diode is $2v_s - 0.7 = 48.6\ V$. To be in the safe side one then need to use diodes with PIV of say $1.5 \times 48.6 = 73\ V$.